

IN THE CLAIMS

Please cancel claim 22 without prejudice to or disclaimer of the subject matter recited therein.

Please amend the claims as follows.

1-4. (Canceled).

5. (Previously amended) A method of stress testing an integrated circuit, comprising:
capturing a first external bus transaction,
if a request type of the transaction matches a triggering condition, generating a data request, and
generating a harassing bus transaction based on the data request.

6. (Original) The method of claim 5, wherein the first external bus transaction and the new external bus transaction are generated by the same integrated circuit.

7. (Original) The method of claim 5, wherein the data request includes an address contained in the first external bus transaction.

8. (Original) The method of claim 5, wherein the external bus transaction includes a first cache line address in a system memory and the data request includes a second cache line address adjacent to the first cache line address.

9. (Previously amended) The method of claim 5, wherein the external bus transaction includes an address directed to a first portion of a cache line in a system memory and the data request includes a second address directed to a second portion of the cache line.

10. (Original) The method of claim 5, wherein the harassing bus transaction is generated before the first external bus transaction concludes.

11-17. (Canceled).

18. (Currently amended) A stress testing method for a computer system, comprising:
counting a number of external bus cycles that occur without onset of a new transaction on the external bus,
determining [when] if the number meets a predetermined threshold,
if so, generating a harassing transaction on the external bus.
19. (Original) The method of claim 18, wherein the harassing transaction includes an address from a previous bus transaction having been modified to refer to an adjacent cache line.
20. (Currently amended) An integrated circuit, comprising:
a processor core, the processor core to operate in the domain of a first clock,
a data request pipeline having an external bus interface that is in communication with an external bus, the external bus to operate in the domain of a second clock, where the second clock is different from the first clock, and
a validation FUB having an input coupled to the external bus interface of the data request pipeline, the validation FUB to operate in the domain of the first clock, the validation FUB further comprising:
a transaction latch coupled to the external bus interface, and
a request library in communication with the transaction latch and having an output coupled to the data request pipeline, and to store transaction request types according to an external bus protocol.
21. (Previously presented) The integrated circuit of claim 20, wherein the first clock is faster than the second clock.
22. (Canceled).
23. (Currently amended) The integrated circuit of ~~claim 22~~claim 20, further comprising an address manipulator coupled to the transaction latch and to the request library.
24. (Previously presented) An integrated circuit, comprising:
a processor core,
a bus sequencing unit in communication with the processor core and an external bus, the bus sequencing unit further comprising:
an arbiter to receive a data request from an external bus transaction,

a cache memory to store data, and
a transaction queue in communication with the arbiter and the cache memory to process the data request, and

a validation FUB in communication with the bus sequencing unit and the external bus, the validation FUB to receive the data request from the arbiter to generate a second data request when the data request matches a triggering condition.

25. (Previously presented) The integrated circuit of claim 24, where an output of the validation FUB is coupled to the arbiter.

26. (Previously presented) The integrated circuit of claim 25, wherein the arbiter processes the data request from the external bus transaction and the second data request as independent transactions.

27. (Previously presented) An integrated circuit, comprising:

a processor core,
a bus sequencing unit in communication with the processor core and an external bus, the bus sequencing unit further comprising:
an arbiter to receive a data request,
a cache memory to output a hit/miss signal in response to the data request,
a transaction queue in communication with the arbiter and the cache memory to process the data request, and

a validation FUB in communication with the bus sequencing unit and the external bus, the validation FUB to receive the hit/miss signal from the cache memory to generate a second data request when the hit/miss signal matches a triggering condition.

28. (Previously presented) The integrated circuit of claim 27, wherein the triggering condition is whether requested data is present in the cache memory.

29. (Previously presented) A diagnostic method for an integrated circuit, comprising:

detecting an onset of a first transaction on an external bus,
reading an address of the first transaction from the external bus, and
in response to the detected transaction, issuing a read request in a second transaction on the external bus, the read request directed to the same address as the first transaction.

30. (Previously presented) The method of claim 29, wherein an onset of the second transaction occurs before the first transaction concludes.
31. (Previously presented) The method of claim 29, further comprising issuing a plurality of read requests directed to addresses of subsequent transactions detected on the external bus.
32. (Previously presented) The method of claim 29, wherein the first and second transactions are issued by the same integrated circuit.
33. (Currently amended) A method, comprising, in a diagnostic mode of the integrated circuit:
detecting a plurality of transactions posted on an external bus if a predetermined condition is met,
reading addresses of the transactions, and
posting a harassing transaction on the external bus for each detected transaction, each harassing instruction including the address of the respective detected transaction.
34. (Previously presented) The method of claim 33, wherein an onset of the harassing transaction occurs before the respective detected transaction concludes.
35. (Previously presented) The method of claim 33, wherein the detected and harassing transactions are issued by the same integrated circuit.
36. (Previously presented) A method of testing an integrated circuit, comprising:
storing a request type in a register,
observing a transaction on an external bus, and
when the request type of the external bus transaction matches the request type stored in the register, generating a data request on the external bus.
37. (Previously presented) the method of claim 36, further comprising generating a harassing bus transaction based on the data request.